The Design Process, Part 1

Setting up the Logic half of the CAD system for design entry

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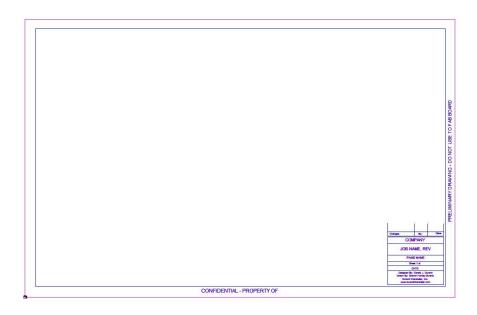
Start with an idea, yours or someone else's. An electronic engineer figures out how to make this idea into a product. He researches the parts needed to come up with a list called the Bill of Materials and decides how to assemble these into the product design. He sketches out the preliminary schematic, a graphic representation of the components and how they are connected together. He then hands it off to the layout designer. The engineer and the designer may be the same person, but not necessarily.

The design software that I use has two distinct parts: Logic, and Layout. Once the schematic is created in Logic, it is linked to the Layout half. This converts all of the graphic representations of the components into the physical "footprint" that will appear on the PC Board. It also relays the connections between the schematic components to the PC Board so that the inter-connectivity is maintained. The connection at this point is not displayed as wires but as a straight line point to point tangle which is referred to as the "rats nest". The two halves of the software can remain linked during layout, though this can cause problems. It is better to link them only when necessary to transmit new information from one to the other.

When starting up a new project, I create a job folder and every part of the job goes into that folder. This keeps everything where it can be easily accessed and in the case of working for a client, it makes it easy to hand over the completed job in an efficient manner.

It is a very good idea to decide on the name of the project early on as renaming the files causes difficulties during the design process. If necessary, a generic name can be used as long as all concerned know what the title refers to. This is especially important when files are handed off to fabrication and assembly houses.

The first part of the layout person's job is to create a schematic page. I have found it very useful to make up a default page that can be reused for further projects.



I have chosen the "B" size format as it can be printed on "A" size paper without too much loss in resolution and can allow for more design space.

Some designers like to use quadrants to break up a page, much like what is used on the borders of maps: alphabetic letters from left to right across the top of the page and numbers along the side from top to bottom. You can do this if you like, but I find it only necessary if you are using a large format of paper where it would be difficult to locate a given part of the design.

The Title Block is an essential part of the page and must appear on every page of the schematic. It contains the following information: the name of the company or individual that owns the rights to the project, the name of the job and its revision number, the name of the page, the number of the page out of the total number of pages, the date of the design's completion (or in the case of a review, the date last changed), who designed the project and who did the layout work.

There are also small sections that indicate changes made after the current revision that may or may not apply to the next revision. These indicate what the change was, who did it and the date of the change. These changes could be any number of things, including that fact that a



particular part is no longer available, something didn't work quite as expected and needed to be corrected, etc. Other information could be added to the Title Block as desired.

I find it helpful to add the following text around the border of each page.

"Confidential - Property of ..." indicating the owner of the design for emphasis and clarity.

And "Preliminary Design - Do Not Use to Fab Board" to prevent this version from being mistaken as the final design. This is most important as schematics are often handed back to the owner of the design for review during the design process and they may mix up versions. The most important reason for this text is that when the layout is complete, the reference designators are re-sequenced for ease of the assembly and debug processes. Of course, this last text is removed when the design is finalized.